GaAs/GaAlAs Heterojunction Bipolar Phototransistor for Monolithic Photoreceiver Operating at 140 Mbit/s

H. WANG, C. BACOT, C. GERARD, J. L. LIEVIN, C. DUBON-CHEVALLIER, D. ANKRI, AND A. SCAVENNEC

Abstract—**The development of optical transmission calls for sensitive and fast optoelectric transducers. With the advent of optical local area networks, hybrid transducers may no longer be appropriate, and monolithic emitters and receivers will be preferred. In this paper, we report on the first monolithic photoreceiver implemented with GaAs–GaAlAs bipolar devices. One phototransistor and two transistors are integrated, together with four resistors on a 0.5×0.5-mm² GaAs chip. The transimpedance receiver has a bandwidth of 80 MHz. Signal and noise power measurements indicate that for a digital signal at 140 Mbit/s, the minimum detectable power is 1 μW (−30 dBm).**

I. Introduction

OPTICAL TRANSMISSIONS on fibers are rapidly developing worldwide. This is exemplified by the development of telecommunications links either for long-distance transmissions or in local area networks (LAN's). These advances derive from the basic advantages of optical fibers over coaxial cable: lower loss, larger bandwidth, and lower weight. This development of optical transmission is also apparent in other areas where noise immunity is important, as in microwaves (sensing, signal distribution to antennas, etc.). Optoelectronic transducers between electrical and optical signals are critical for the development of optical transmission, and the integration of high-speed electronic signal processing circuits with optoelectronic devices offers a potentiality which can be paralleled with the impact of silicon circuit integration in computer science. Unfortunately, optoelectronic and electronic devices usually have structures which make monolithic integration difficult to envision. In that respect, the heterojunction bipolar transistors and phototransistors show great promise since they have the same basic structure.

The heterojunction phototransistor (HPT), which behaves like a photodiode driving a bipolar transistor, has already been widely studied, and its sensitivity has been shown to be comparable to that of avalanche photodiodes (APD) or photoreceivers associating a p-i-n photodiode and a GaAs MESFET (p-i-nFET), for a bandwidth of the order of 1 GHz [1]. A figure of merit $\sqrt{g_m}/C_{\text{input}}$ is actually used to qualify the ability of a receiver to have a high sensitivity. Heterojunction bipolar phototransistors with a diffused structure have been developed in our laboratory (Fig. 1), resulting in high-current-gain, low-capacitance devices. Such characteristics result in large signal-to-noise ratios under weak illumination, and in an extension of the interesting range of application of HPT's to bit rates around 140 Mbit/s and above.

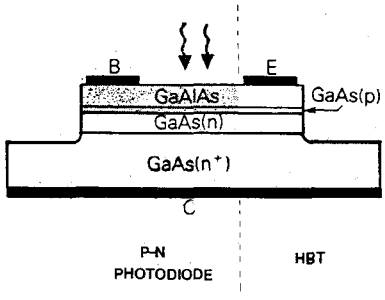

Fig. 1. Diffused-structure phototransistor. The right part can be considered a p−n photodiode and the left part a low-input-capacitance heterojunction bipolar transistor driven by the photodiode.

In this paper, we present the design, fabrication technology, and experimental results of the first monolithic photoreceiver integrating heterojunction bipolar devices. Accurate optical and microwave characterizations are performed, and the comparison to theoretical results illustrates the main physical parameters involved in improving the sensitivity.

II. Design

The monolithic photoreceiver presented in this paper is integrated on a 0.5×0.5-mm² GaAs chip. The circuit comprises one HPT, two heterojunction bipolar transistors (HBT's), and four resistors [Fig. 2]. The layout of the circuit is based on heterojunction bipolar technology with 4-μm design rules. The first objective of this work was to realize a high-sensitivity, high-stability monolithic photoreceiver for LAN communication links at 0.85-μm wavelength, before possible extension of this technology to higher bit rates (for computer interconnects, for instance).

From extensive simulation and optimization, we reached the following conclusions.

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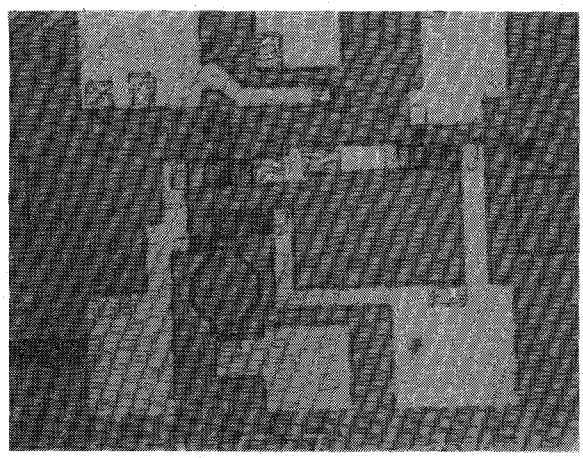
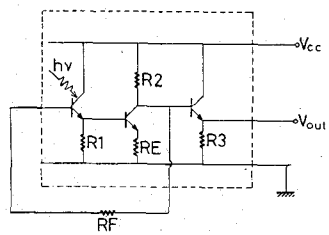


(a)



(b)

Fig. 2. (a) Microphotograph of the monolithic photoreceiver. (b) Circuit diagram of the monolithic photoreceiver.

layer	dopant	concentration	Al	thickness
cap	Si	Max	0	3000 A
emitter	Si	2E17	0.3	3000 A
	Si	graded	graded	300 A
base	Be	2E18	0	1000 A
collector	Si	3E15	0	19000 A
buffer	Si	2E18	0	10000A
	Substrate (semi-insulating)			

(a)

layer	dopant	concentration	Al	thickness
cap	Si	4E18	0	2600 A
emitter	Si	5E17	0.3	4200 A
	Si	graded	graded	500 A
base	Be	8E17	0	500 A
collector	Si	3E16	0	10500 A
buffer	Si	2E18	0	10000A
	Substrate (semi-insulating)			

(b)

Fig. 3. Multilayer structures for monolithic photoreceiver. (a) Optimized structure. (b) Structure used in this work.

1) The diffused-structure HPT with a base contact has been preferred because of its lower input capacitance and higher responsivity than conventional structures, and because of the reduction of the falling tail in the time-domain pulse response, as compared to noncontacted base devices.

2) As LAN links require high stability and large dynamic range, the transimpedance configuration has been preferred for the receiver to the high-impedance design, which is known to have a limited dynamic range.

3) The digital receiver sensitivity is usually measured in terms of the minimum detectable power for a given bit rate and a bit error rate of 10^{-9}. The sensitivity of diffused HPT's with base contact has been analyzed elsewhere [3], [7]. For a given processing technology, the sensitivity depends on the multilayer structure. Optimization of the multilayer structure can be summarized as follows: a thin base layer ($\simeq 1000$ Å) and thick collector layer ($\simeq 2$ μm) with a low doping level are required for high current gain and high responsivity, respectively, without introducing significant base access resistance and collector depletion layer transit time. The optimized multilayer structure and the one we have actually used are shown in Fig. 3(a) and (b), respectively.

4) Different structures of the three-stage receiver have been compared by simulation. The dominant pole is determined by the RC time constant of the input impedance; the receiver with the input HPT in a common-collector configuration has shown a larger bandwidth, which corresponds to the elimination of the Miller effect, compared to the common emitter. For that reason, HPT in the common-collector configuration has been retained for this work.

5) The stability of the circuit is ensured by the series resistor R_E (Fig. 2(b)). This resistor also helps to lower the dependence of the circuit characteristics on the dispersion of integrated resistor values and HBT and HPT parameters (f_T, β, etc.) [4].

6) The dc coupling is retained so that different modulation schemes can be used without any limitation.

7) The photosensitive area of the HPT has an equivalent diameter of 56 μm, compatible with the core dimension of multimode fibers.

8) At the present stage of fabrication, the feedback resistor R_f is not integrated on the GaAs chip. This comes from its resistance value, which is much higher than for the other resistors.

The simulation results of this circuit have shown that, with an optimized multilayer structure, a minimum detectable power of -40 dBm is achievable at a data rate of 140 Mbit/s [4]. Using the same HPT structure and circuit design, the simulation for an improved technology (2-μm self-aligned technology and integrated feedback resistor) gives a minimum detectable power of -35 dBm for a 1-Gbit/s data rate with a bit error rate of 10^{-9}.

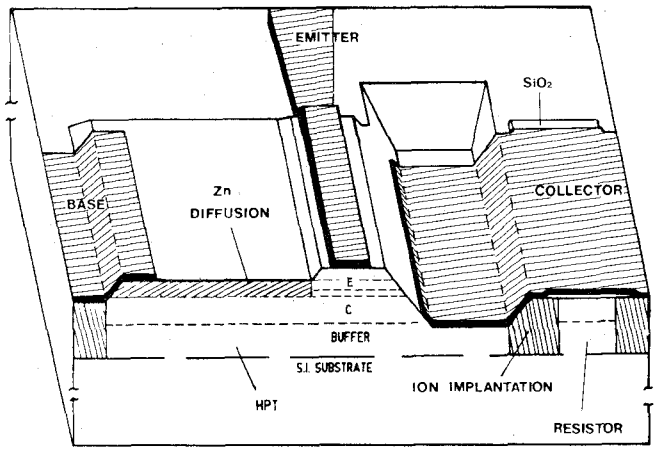


Fig. 4. Perspective view of an HPT with an integrated resistor delimited by ion implantation in the buffer and the collector layer.

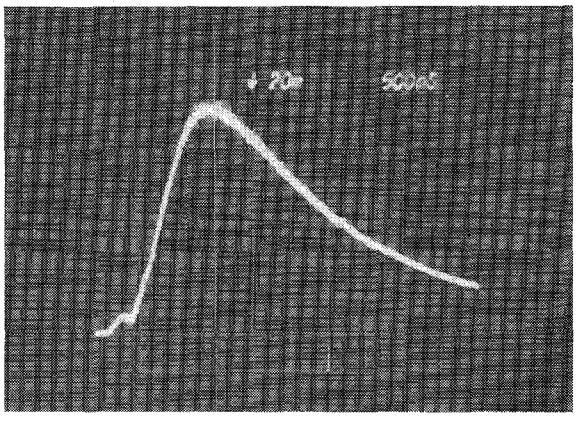


Fig. 5. Optical pulse response of the monolithic photoreceiver.

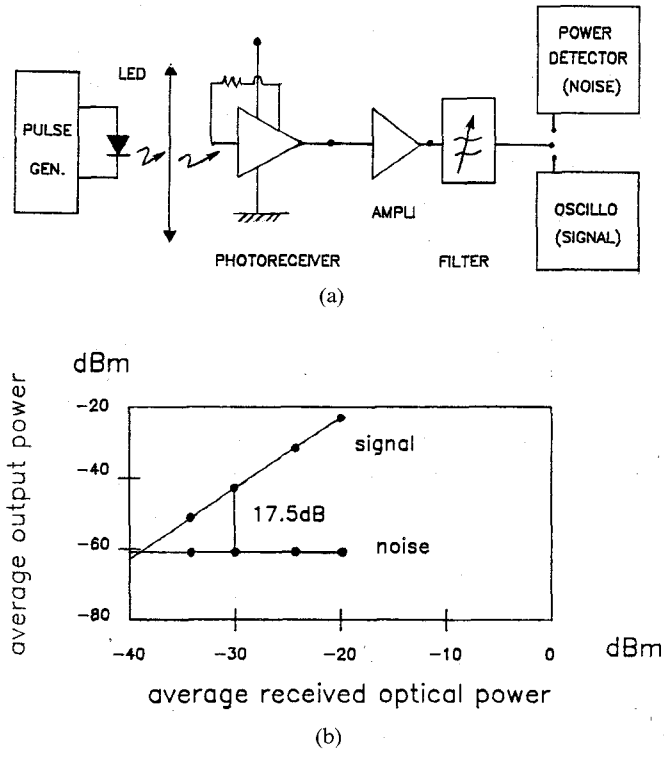


Fig. 6. (a) Signal-to-noise measurement. (b) Measured signal-to-noise ratio.

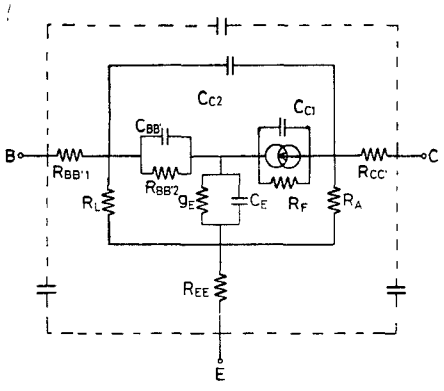
III. Fabrication Technology

The multilayer structure was grown by molecular beam epitaxy. Very high current gain, up to 3000, has been obtained on bipolar transistors with similar epitaxial structures [4] (Fig. 3(b)). The fabrication process for a multilayer wafer includes the following steps [Fig. 4]: a) emitter mesa etching to eliminate the GaAs emitter contact layer; b) localized Zn diffusion to reach the base layer for base contact and to convert most of the emitter layer of the HPT to p-type (diffused structure [2]); c) base mesa etching to eliminate the base layer outside the active area; d) H^+ and B^+ implantation for isolation; e) collector via-hole etching to reach the n^+ buffer layer; f) dielectric (SiO_2) deposition for isolation between resistor and metal line; g) n-type contact; h) p-type contact; i) interconnection deposition; and j) antireflection coating deposition.

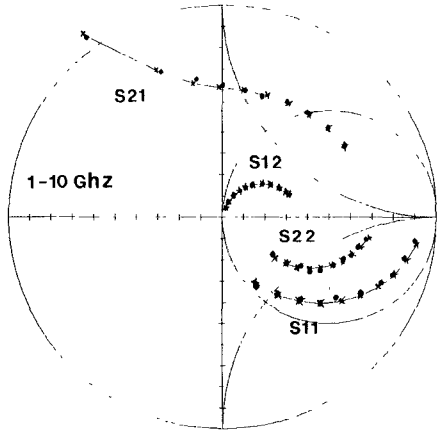
The isotropic etching of GaAs and GaAlAs is performed by wet processing using H_2O–H_2O_2–H_3PO_4 (40:1:3). The diffusion is conducted in a sealed tube at 630°C with Si_3N_4 as a mask. In order to define accurately the active area during isolation by ion implantation, gold is used for masking instead of photoresist. The p-region and n-region contacts are made with AuMn [5] and AuGeNi, respectively. The SiO_2 film deposited by UV-enhanced CVD for the antireflection coat layer is also used to passivate the circuit surface. In this process, the integrated resistors are delimited by implantation in the buffer layer.

IV. Experimental Results

The monolithic photoreceiver with a 26-kΩ external feedback resistor operates from a single 7-V supply voltage. The transimpedance gain has been measured as 7000 V/A, and noise measurements with a low-pass filter of 70 MHz have shown a noise equivalent power (NEP) of −61 dBm at the output. The measured NEP results mainly from the input HPT noise and does not depend on the incident optical power as long as it is in the microwatt range, in contrast with the high-input impedance p-i-nFET photoreceiver. This is because the phototransistor base bias current is relatively large (27.5 μA) compared with the photocurrent, so that the shot noise of the optical current does not contribute significantly to the total noise. A pulse measurement using a GaAs laser operating at 0.82 μm and emitting optical pulses of less than 100-ps duration has been performed (Fig. 5); the exponential trailing edge has a time constant of 2 ns, which corresponds to a first-order pole of the transfer function of 80 MHz. The Fourier transform computation of this pulse response exhibits a bandwidth larger than 80 MHz (close to 100 MHz, actually) with a 6-dB rolloff, showing that the transfer function has a well-defined single pole in that frequency range, as expected from simulations. Optical measurements conducted at a few MHz with a 0.85-μm LED have shown an electrooptical gain of 1500 V/W for the receiver. From the combined experimental results on signal and noise power



(a)



(b)

Fig. 7. (a) Equivalent circuit of the HBT. (b) *S*-parameters measured and calculated from the equivalent circuit of HBT.

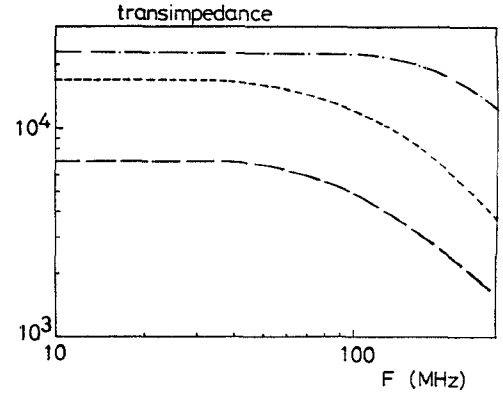


Fig. 8. Comparison of gain–bandwidth performance. —— Simulation using equivalent circuit obtained by parameter extraction from *S*-parameter on experimental device. - - - - - - - - Simulation without Early effect and contact resistance. ——— Simulation without Early effect and contact resistance, using the optimized multilayer structure (lower base resistance, lower collector capacitance, higher current gain).

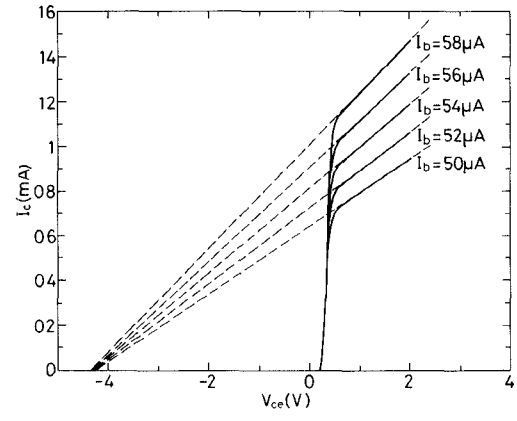


Fig. 9. Early voltage of the HBT used in this circuit.

at the output, one can infer the variations of signal-to-noise ratio versus input optical power (Fig. 6). This, together with the measured bandwidth of the receiver, leads to an estimated sensitivity for the receiver of −30 dBm at a 140-Mbit/s transmission rate for an error rate of 10^{-9} [6].

V. Electrical Characterization and Comparison of Experimental Results to Theory

S-parameter measurements have been carried out on discrete devices (HBT and HPT) located in a test area of the same wafer. Transition frequencies larger than 8 GHz for the HBT and close to 2 GHz for the HPT have been obtained. These measurements are performed with an extended de-embedding technique which makes it possible to reduce the parasitics of the test fixture to less than 0.1 dB. From these measurements, the electrical equivalent circuits of HPT and HBT have been established by a CAD program (Fig. 7).

It appears that if low junction capacitances are effectively obtained, relatively high series resistances are observed for the emitter ($R_E = 35\ \Omega$) and for the collector ($R_C = 40\ \Omega$). Contact resistivity higher than expected ($\rho_c = 4.5 \times 10^{-5}$) seems to be at the origin of this high resistance value. TLM measurements on test structures have since confirmed this observation. Simulations of the electrical circuit of the photoreceiver have led to a transimpedance gain of 3×10^6 V/A MHz [3]; the difference with the experimentally measured 5.6×10^5 V/A MHz has been studied using the electrical equivalent circuits of HPT's and HBT's. The use of a nonoptimum multilayer structure has resulted in an increase in the collector capacitance and base resistance. This in turn is the reason for the lower than expected values for both the transition frequencies and transimpedance gain. Also, the Early effect, which had been neglected in our earlier simulation, tends to decrease the transimpedance gain (Fig. 8). This effect, not taken into account in our previous model, is particularly important in the fabricated phototransistor because of the low base doping level. The Early voltage of HBT and HPT is about 4 V (Fig. 9). The ultimate sensitivity performance of this photoreceiver if fabricated with lower contact resistance and higher quantum efficiency would be close to −40 dBm for a 140-Mbit/s data rate.

VI. Conclusions

The first monolithic photoreceiver implemented with HPT has been fabricated and tested. The experimental results show that by taking advantage of the compatibility between HBT and HPT, a monolithic photoreceiver with

heterojunction bipolar devices can achieve high reliability and low parasitic noise. Although the performance obtained is already among the best reported on monolithic photoreceivers at 0.85 μm, improvements in available technology will lead to a higher sensitivity and higher gain–bandwidth product.

Acknowledgment

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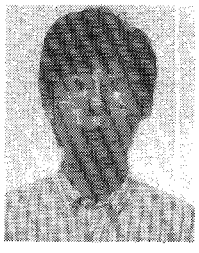

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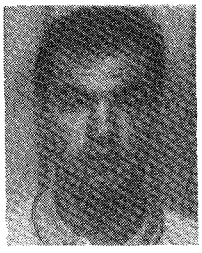

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